ABDULLAH SAHRURI

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EDUCATION

University of Louisiana at Lafayette — Lafayette, LA
Ph.D. Computer Engineering (CGPA: 3.85) — 2023 - (Expected Grad. 2026)
Academic advisor: *Martin Margala*
Relevant Coursework: Analog VLSI Design • VLSI Structures • Computer Arithmetics • VLSI Testing • Design and Analysis of Algorithms • Principles of Computer Architecture • Computer Design and Implementation • Principles of Programming Languages

Yeditepe University — Istanbul, Turkey
M.S. Electrical and Electronics Engineering (CGPA: 3.93) — 2019 - 2022
Thesis: High Fan-in Differential Capacitive-Threshold-Logic Implementation With an Offset-Compensated Comparator: Designed a novel high fan-in threshold logic gate suitable for fast data-intensive computations. The design uses a capacitive feedback loop, minimum-sized MOSFET capacitors, and digital logic levels for programming the gate to a desired complex function. The gate operates in two phases: evaluation and reset. Analyzed five gates of fan-ins 31, 63, 127, 255, and 511, and validates the design using 65nm CMOS technology.
Academic advisor: *Ugur Cilingiroglu*
Relevant Coursework: Analog IC Design • RF Circuit Design • Advanced Electronics • Sensors • Advanced Communication Systems • Advanced Control Systems • Advanced Robotic Systems

Yeditepe University — Istanbul, Turkey
B.S. Electrical and Electronics Engineering (CGPA: 3.25) — 2014 - 2019
Graduation Project: Designed a Lead-compensated Miller OTA as a single-supply (V_{DD} = 1.2 V) unity-gain buffer amplifier using 90nm CMOS technology. The OTA achieves an open-loop voltage gain of A_0 = 53.2 dB at V_0 = 0.45 V using a beta-multiplier current reference. Simulated results from Cadence Virtuoso verify that the unity-gain amplifier settles with a phase margin of no less than 65° and a settling time of 34 ns for a 0.03% settling error.
Academic advisor: *Ugur Cilingiroglu*
Relevant Coursework: Analog IC Design • High Frequency Electronics • Physical Design Of IC • Digital IC Design • Analog Electronic Circuits • Microprocessor Systems • Coding And Information Theory • Wireless Communication • Antennas and Propagation

TECHNICAL SKILLS

Programming

C • TCL • Python • Linux • HDL (Verilog, VerilogA, SystemVerilog, VHDL) • MATLAB

Computer-Aided Design

Cadence Virtuoso (Analog/Mixed Signal Circuit Design, First Encounter, Innovus, DRC, LVS, QRC) • Cadencec SKILL • Liberate • Cadence AWR (RF Circuit Design, Layout, EM Simulation) • SPICE • HSPICE • Spectre

WORK EXPERIENCE

Memory Circuit Design Intern

Broadcom Austin, TX
Full-Time Internship May 2024 - August 2024

Latch Characterization: Conducted detailed latch characterization across different process corners, focusing on advanced node technologies • Scripting and Automation: Developed and optimized TCL scripts for layout placement, improving the efficiency of the design process • Design Flow Development: Created a comprehensive design flow using Python, enhancing the automation of characterization and validation processes • Collaboration and Communication: Presented and discussed progress in project-related meetings, working closely with cross-functional teams • Technologies and Tools: Gained hands-on experience with Python, TCL, Advanced Node CMOS technology, Characterization flows, and Static Timing Analysis (STA).

Research Assistant

University of Louisiana at Lafayette Lafayette, LA
Full-Time 2023 - Present (2027)

Research experience in the field of Hardware Security and VLSI Testing. Reviewed papers in VLSI and Analog/Mixed-Signal Integrated Circuits. Created circuits and layouts in Cadence Virtuoso for publications.

PUBLICATIONS

A. G. Ayar, **A. Sahruri**, S. Aygun, M. S. Moghadam, M. H. Najafi and M. Margala, "Detecting Vulnerability in Hardware Description Languages: Opcode Language Processing," in *IEEE Embedded Systems Letters*, doi: 10.1109/LES.2023.3334728.

A. Sahruri, M. Margala, U. Cilingiroglu. "HiCTL: High Fan-in Differential Capacitive-Threshold-Logic Gate Implementation With An Offset-Compensated Comparator". *25th International Symposium on Quality Electronic Design (ISQED)*, San Francisco, CA, USA, 2024, pp. 1-7, doi:10.1109/ISQED60706.2024.10528704.

POSTER PRESENTATIONS

16th Dallas Circuits and Systems Society (DCAS). *"High Fan-in Differential Capacitive-Threshold-Logic Implementation With an Offset-Compensated Comparator"* April 2023, Dallas, TX. [Best Poster Award]

IBM IEEE CAS/EDS – AI Compute Symposium, *"A 32-bit Neuromorphic ALU Based on Threshold Logic Gates."* November 2023, IBM T.J. Watson Research Center, Yorktown Heights, New York

PROFESSIONAL MEMBERSHIPS

Institute of Electrical and Electronics Engineers (IEEE)
Reviewer of ISCAS in the following tracks: 1) Design and Verification of Digital Integrated Circuits and Systems 2) Electronic Design Automation and Physical Design 3) Low-Power Logic Circuits and Architectures

Association for Computing Machinery (ACM)